VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

The paragraph at page 10, lines 5-14 has been amended as follows:

FIGS. 1A and **1B** are top and bottom perspective views, respectively, of semiconductor chip 110 which is an integrated circuit in which various transistors, circuits, interconnect lines and the like are formed (not shown). Chip 110 includes opposing major surfaces 112 and 114 and has a thickness of 200 microns between these surfaces. Surface 112 is an upper surface, and surface 114 is a lower surface. Surface 112 is the active surface and includes conductive pads 116 arranged in a single row and passivation layer 118. Pads 116 are substantially aligned with passivation layer 118 so that surface 112 is essentially flat. Alternatively, if desired, pads 116 can extend above or be recessed below passivation layer 118. Pads 116 provides bonding sites to electrically couple chip 110 with external circuitry. Thus, a particular pad 116 can be input/output pad or a power/ground pad. Pads 116 have a length and width of 70 microns.

The paragraph at page 16, lines 10-13 has been amended as follows:

FIG. 5C is an enlarged plan view of encircled detail 5C in FIG. 5A that shows a representative pad 116 and routing line 148 in greater detail. Since pad 116 and routing line 148 are not ~~be~~ visible from surface 114 of chip 110, they are shown in phantom. Routing line 148 includes a distal end that overlaps pad 116.

The paragraph at page 19, lines 27-31 has been amended as follows:

A suitable wet chemical etch can be provided by the same solution used to form slots 128 and recessed portions 130, 132 and 134. The optimal etch time for exposing the structure to the wet chemical etch without excessively exposing the portions of leads 138 embedded in peripheral portion 166 and adjacent to inner side surfaces 174 **after** the selected copper has been removed can be established through trial and error.

The paragraph at page 23, line 23 to page 24, line 6 has been amended as follows:

At this stage, device 186 includes chip 110, conductive traces 150, adhesive 154, connection joints 180 and insulative housing 184. Conductive traces 150 each include a lead 138 that protrudes laterally from **and** extends through a side surface 162 of insulative housing 184, a terminal 146 that protrudes downwardly from and extends through bottom surface 164 of insulative housing 184, and a routing line 148 within insulative housing 184 that is integral with an associated terminal 146 and contacts an associated lead 138 and connection joint 180. Conductive traces 150 are electrically connected to pads 116 by connection joints 180 in one-to-one relation, and are electrically isolated from one another. Leads 138 are arranged in opposing rows that protrude laterally from and extend through opposing side surfaces 162 and are disposed between top surface 160 and bottom surface 164. Terminals 146 are arranged as an array that protrudes downwardly from and extends through bottom surface 164 and is disposed inside inner side surfaces 174. Furthermore, leads 138 and terminals 146 are spaced and separated from one another outside insulative housing 184, and leads 138 and terminals 146 are electrically connected to one another and to pads 116 inside insulative housing 184 and outside chip 110.

The paragraph at page 25, lines 16-24 has been amended as follows:

Advantageously, the present invention provides a semiconductor package device that has ~~have~~ a first electrode configuration for the test socket and a second electrode configuration for the next level assembly. The first electrode configuration is provided by the leads, and the second electrode configuration is provided by the terminals. As a result, the device is flexible enough to accommodate test sockets and printed circuit boards with different electrical contact requirements. In other words, the leads can be optimized for mating with the test socket, and the terminals can be optimized for mating with the next level assembly. In this manner, the device can be tested using a standard test socket, and then attached to a printed circuit board with an entirely different contact arrangement than the test socket.

The paragraph at page 30, line 22 to page 31, line 9 has been amended as follows:

The connection joints can be formed from a wide variety of materials including copper, gold, nickel, palladium, tin, alloys thereof, and combinations thereof, can be formed by a wide variety of processes including electroplating, electroless plating, ball bonding, solder reflowing and conductive adhesive curing, and can have a wide variety of shapes **and**~~as~~ sizes. The shape and composition of the connection joints depends on the composition of the conductive traces as well as design and reliability considerations. Further details regarding an electroplated connection joint are disclosed in U.S. Application Serial No. 09/865,367 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Simultaneously Electroplated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding an electrolessly plated connection joint are disclosed in U.S. Application Serial No. 09/864,555 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding a ball bond connection joint are disclosed in U.S. Application Serial No. 09/864,773 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Ball Bond Connection Joint" which is incorporated by reference. Further details regarding a solder or conductive adhesive connection joint are disclosed in U.S. Application Serial No. 09/927,216 filed August 10, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Hardened Connection Joint" which is incorporated by reference.

The paragraph at page 32, lines 18-22 has been amended as follows:

For instance, if an optoelectronic chip is employed with a light sensitive cell and pads on the upper surface, the pads, adhesive, conductive traces and connection joints are disposed outside the light sensitive cell, and the insulative base is a transparent epoxy layer that is deposited on the light sensitive cell, then the light sensitive cell will **receive**~~be exposed to~~ light from the external environment that impinges upon and passes through the insulative base.

In the Claims

The claims have been amended as follows:

1. (Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces**, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion**;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein **the first single-piece housing portion contacts the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal,** the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

2. (Amended) The device of claim 1, wherein the **first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface**~~insulative housing includes a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal~~.

3. (Amended) The device of claim ~~1~~**2**, wherein the first single-piece housing portion contacts the lower surface.

4. (Amended) The device of claim ~~12~~, wherein the insulative housing consists of the first and second single-piece housing portions.

11. (Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces**, wherein the insulative housing consists of a first single-piece housing portion and a second single-piece housing portion**;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a terminal that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein **the first single-piece housing portion contacts the lower surface and the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal,** the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

12. (Amended) The device of claim 11, wherein the **first single-piece housing portion is farther from the top surface than the lower surface is from the top surface**~~insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal~~.

13. (Amended) The device of claim 11~~2~~, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the

second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

15. (Amended) The device of claim 11~~2~~, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

16. (Amended) The device of claim 11~~2~~, wherein the second single-piece housing portion includes first and second opposing surfaces, the first surface contacts the lead and the second surface provides a portion of the bottom surface.

31. (Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a terminal that protrudes downwardly from and extends through the central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad, wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance; and

a lead that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

41. (Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that **contacts and** extends **into the insulative housing** ~~through the side surface~~ and is spaced from the top and bottom surfaces **and does not overlap the chip** and a non-recessed portion that **contacts and** extends outside the insulative housing and is adjacent to the recessed portion and ~~a corner between the side surface and~~ the bottom surface, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

51. (Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a terminal that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion ~~inside the insulative housing~~ that **contacts and** extends **into the insulative housing** ~~through the side surface~~ and is spaced from the top and bottom surfaces **and does not overlap the chip** and a non-recessed portion **that**

contacts and extends outside the insulative housing **and** ~~that~~ is adjacent to ~~and integral with~~ the recessed portion and ~~contacts the side surface and is adjacent to a corner between the side surface and~~ the bottom surface, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Claims 61-120 have been added.

REMARKS

Claim 1-120 are pending. In this Response, claims 1-4, 11-13, 15, 16, 31, 41 and 51 have been amended, and claims 61-120 have been added.

I. DRAWING OBJECTIONS

The drawings are objected to under 37 C.F.R. § 1.83(a) since the drawings must show every feature of the invention specified in the claims, and therefore various features must be shown or canceled from the claims.

The Examiner asserts that the limitation in claims 7, 17, 28,47 and 57 "the terminal is within a periphery of the chip, and the lead is outside the periphery of the chip" is not shown in the drawings. This is clearly erroneous.

Chip 110 is illustrated in Figs. 1A and 1B. Lead 138 that extends outwardly from central portion 126 between slots 128 and includes recessed portion 132 and non-recessed portion 136 is shown in Figs. 2A and 2B. Metal trace 144 that includes terminal 146 and routing line 148 is shown in Figs. 3A and 3B.

Chip 110 is mechanically attached to metal base 120 by adhesive 154 in Figs. 5A and 5B. Lead 138 is shown outside the periphery of chip 110 in Fig. 5A. Although lead 138 is not labeled in Fig. 5A, its identification is clear in view of Fig. 2A. Terminal 146 is shown within the periphery of chip 110 by comparing Figs. 3A and 5A. Terminal 146 cannot be labeled in Fig. 5A since it is not visible. Although another figure could be added that shows chip 110 and terminal 146 in phantom, the fact that terminal 146 is within the periphery of chip 110 is sufficiently clear by comparing Figs. 3A and 5A.

Furthermore, lead 138 is shown outside the periphery of chip 110 and terminal 146 is shown within the periphery of chip 110 in Figs. 6D and 7D. Although lead 138 is not labeled in Figs. 6D and 7D, its identification is clear from Figs. 2B and 2G. Although terminal 146 is not labeled in Figs. 6D and 7D, its identification is clear from Fig. 4C.

Figs. 2F, 2G and 2H are enlarged cross-sectional views showing the formation of recessed portion 132 taken across line 2F—2F in Figs. 2A and 2B, Fig. 4C is an enlarged cross-sectional view taken across line 4C—4C in Fig. 4A, Fig. 6D is an enlarged cross-sectional view taken across line 6D—6D in Fig. 6A, and Fig. 7D is an enlarged cross-sectional view taken across line 7D—7D in Fig. 7A.

Thus, the identification of lead 138 in Figs. 2A, 4C, 6D and 7D, and the identification of terminal 146 in Figs. 6D and 7D would be apparent to those skilled in the art. Moreover, the fact that lead 138 is outside the periphery of chip 110 and terminal 146 is within the periphery of chip 110 in Figs. 6D and 7D would be apparent to those skilled in the art.

However, in the interests of expediting the case, the Submission Of Proposed Drawing Amendment For Approval By Examiner filed concurrently herewith proposes labeling lead 138, metal trace 144 and terminal 146 in Figs. 6D and 7D.

Therefore, Applicant requests that these objections be withdrawn.

II. SECTION 112, FIRST PARAGRAPH REJECTIONS

Claims 7, 17, 28, 47 and 57 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The Examiner asserts that the Specification fails to disclosure a terminal being within a periphery of the chip and a lead being outside the periphery of the chip. This is clearly erroneous.

Figs. 5A, 6D and 7D show terminal 146 within the periphery of the chip 110 and the lead 138 outside the periphery of the chip 110, as explained above for the drawings.

The Specification illustrates terminal 146 within the periphery of the chip 110 and the lead 138 outside the periphery of the chip 110:

> Chip 110 and metal base 120 are positioned relative to one another so that chip 110 is disposed within the periphery of adhesive 154, terminals 146 are disposed within the periphery of chip 110 between pads 116 and the outer edges of chip 110, routing lines 148 extend within and outside the periphery of chip 110 and overlap and are electrically isolated from pads 116, and slots 128, recessed portions 132 and 134, non-recessed portions 136 and leads 138 are disposed outside the periphery of chip 110. (Page 15, lines 24-29.)

The Examiner also asserts that the Specification fails to disclosure the lead being electrically connected to a pad without wire bonds, TAB leads or solder joints, and specifically it cannot be determined how the lead is electrically connected to the pad. This is clearly erroneous.

The Specification illustrates that conductive trace 150 includes lead 138 and metal trace 144, that metal trace 144 includes terminal 146 and routing line 148, and that connection joint 180 contacts and electrically connects pad 116 and routing line 148:

> Metal traces 144 include terminals 146 and routing lines 148. Terminals 146 are formed in recessed portions 130, extend into metal base 120 and protrude below routing lines 148. Terminals 146 are bumped and include cavities that extend into and face away from recessed portions 130. Routing lines 148 are formed outside recessed portions 130 and extend from terminals 146 to leads 138. More particularly, routing lines 148 extend to recessed portions 132 where they are centered between the adjoining slots 128 but do not extend to non-recessed portions 136. Routing lines 148 also extend from terminals 146 towards the inside of central portion 126 in the opposite direction. Thus, each metal trace 144 includes a terminal 146 in a corresponding recessed portion 130 and a routing line 148 that (1) extends from the terminal 146 to a corresponding lead 138, and (2) extends from the terminal 146 in the opposite direction towards the inside of central portion 126. Accordingly, leads 138 and metal traces 144 are formed in one-to-one relation. Conductive traces 150 include leads 138 and metal traces 144. (Page 13, lines 4-16.)

> Connection joints 180 are formed in openings 176 and contact pads 116 and routing lines 148, thereby electrically connecting pads 116 and routing lines 148. (Page 21, lines 11-12.)

> Conductive traces 150 each include a lead 138 that protrudes laterally from extends through a side surface 162 of insulative housing 184, a terminal 146 that protrudes downwardly from and extends through bottom surface 164 of insulative housing 184, and a routing line 148 within insulative housing 184 that is integral with an associated terminal 146 and contacts an associated lead 138 and connection joint 180. Conductive traces 150 are electrically connected to pads 116 by connection joints 180 in one-to-one relation, and are electrically isolated from one another. (Page 23, lines 24-30.)
>
> Furthermore, since leads 138 are electrically connected to pads 116 by routing lines 148 and connection joints 180, and terminals 146 are integral with routing lines 148, it is not necessary for test socket 188 to electrically contact terminals 146. (Page 25, lines 28-31.)

The Specification also illustrates metal trace 144 is formed on lead 138 by an electroplating operation, and connection joint 180 is formed on pad 116 and routing line 148 by ball bonding:

> Metal trace 144 is formed in the opening in photoresist layer 152 and on the exposed portion of surface 122 by an electroplating operation using photoresist layer 152 as a plating mask. (Page 14, lines 12-13.)
>
> The combination of heat, pressure and ultrasonic vibration places the wire ball in a soft state which is easy to deform and forms a ball bond that contacts and is metallurgically bonded to pad 116 and routing line 148. (Page 21, lines 21-24.)

Thus, conductive trace 150 includes lead 138, which is an unetched portion of metal base 120 (and may include plated protective coating 170), and metal trace 144, which is an electroplated nickel/copper/nickel tri-layer. Connection joint 180 is a ball bond, which is not a wire bond as the term is understood by those skilled in the art. See U.S. Application Serial No. 09/864,773 filed May 24, 2001 (incorporated by reference at page 31, lines 3-6).

The Specification also makes clear that a wide variety of connection joints can be employed without wire bonding, TAB leads or solder joints:

> The connection joints can be formed from a wide variety of materials including copper, gold, nickel, palladium, tin, alloys thereof, and combinations thereof, can be formed by a wide variety of processes including electroplating, electroless plating, ball bonding, solder reflowing and conductive adhesive curing, and can have a wide variety of shapes as sizes. The shape and composition of the connection joints depends on the composition of the conductive traces as well as design and reliability considerations. Further details regarding an electroplated connection joint are disclosed in U.S. Application Serial No. 09/865,367 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Simultaneously Electroplated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding an electrolessly plated connection joint are disclosed in U.S. Application Serial No. 09/864,555 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding a ball bond connection joint are disclosed in U.S. Application Serial No. 09/864,773 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Ball Bond Connection Joint" which is incorporated by reference. Further details regarding a solder or conductive adhesive connection joint are disclosed in U.S. Application Serial No. 09/927,216 filed August 10, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Hardened Connection Joint" which is incorporated by reference. (Page 30, line 22 to page 31, line 9.)
>
> Furthermore, the conductive traces can be mechanically and metallurgically coupled to the chip without wire bonding, TAB or solder joints, although the process is flexible enough to accommodate these techniques if desired. (Page 34, lines 20-22.)

Therefore, Applicant requests that these rejections be withdrawn.

III. SECTION 102 REJECTIONS

Claims 1, 5-11 and 17-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Shin et al.* (U.S. Patent No. 5,405,809).

Shin et al. addresses lead end grid array semiconductor package size reduction:

> However, such a conventional quad flat semiconductor package is difficult to reduce in size because the leads are in the same plane as the plastic encapsulating part and extend from the four sides of the package to the exterior. In addition, the high integration of semiconductor chips requires an exceptionally increased number of pins the distance between which has been technically difficult to narrow to a certain value. Thus, to accommodate a large number of pins, a large-sized package is necessary, which results in retrogradation against the tendency toward the small size of semiconductor packages. (Col. 1, lines 34-43.)

Shin et al. solves the problem by bending a lead frame so that the leads include a different plane direction-converting lead part, an identical plane direction-converting lead part, and a bending part therebetween. The leads ends are distributed as a grid array. Furthermore, the grid array is as small as or similar to the area of the semiconductor chip.

> Therefore, it is an objective of the present invention to provide a grid array type lead frame in which the package area is reduced similar to the size of a semiconductor chip while the exposed lead ends used as input and output ends are increased in the number per area, and a lead end grid array semiconductor package utilizing such a lead frame. (Col. 2, lines 47-52.)
>
> It is a further objective of the present invention to provide a grid array type lead frame in which the exposed lead ends with an increased number per area are farther distant from each other while the package area is reduced similar to the size of a semiconductor chip, and a lead end grid array semiconductor package utilizing such a lead frame. (Col. 2, lines 53-60.)

> More particularly, the present invention relates to a grid array type lead frame having a plurality of leads classified into groups by length, in each of which at least one different plane direction-converting lead part and/or at least one identical plane direction-converting lead part is formed by at least one bending part, thereby distributing leads ends in a grid array, and a lead end grid array semiconductor package employing the same, which is as small as or similar to that of a semiconductor chip in area . . . (Col. 1, lines 9-17.)

Shin et al. discloses grid array type lead frame 1 which includes leads 2 and chip pad 5.

Leads 2 include direction-converting lead parts 2a and 2b, first and second bending parts 3 and 3a, and lead ends 4. Direction-converting lead parts 2a and 2b are introduced into different planes by first and second bending parts 3 and 3a, respectively. Different plane direction-converting part 2a is slant bent to the XY axis and the XZ axis by first bending part 3, and different plane direction-converting part 2b is bent to the X axis and the Y axis by second bending part 3a.

Leads 2 are bent to the X axis and/or Y axis, and the Z axis, and extend to the same plane below the semiconductor chip mounting area where lead ends 4 form a grid array. Each lead end 4 includes lead prominence 4' used as an input and output terminal after completion of the semiconductor package fabrication.

A semiconductor chip is attached to chip pad 5 by an adhesive such as epoxy resin or tape. Thereafter, a liquid of encapsulating resin is molded into a plastic encapsulating part that surrounds the chip.

In Fig. 10A, lead end grid array semiconductor package 10α includes lead 2 extending to lead end 4 with prominence 4', semiconductor chip 20 mounted on chip pads 5' by an adhesive such as epoxy resin or tape, bond wire 30 that electrically connects lead 2 to chip 20, and plastic encapsulating part 40 that protects lead 2, chip 20 and bond wire 30 from the external environment. Lead end 4 protrudes from the bottom of plastic encapsulating part 40, and prominence 4' is an input and output terminal distributed in a grid array.

In Fig. 10B, lead end grid array semiconductor package 10β is a modified version of package 10α in which chip 20 is inverted and lead 2 is electrically connected to chip 20 by solder joint 31 rather than bond wire 30. Alternatively, lead 2 can be electrically connected to chip 20 by a bond wire.

Claim 1 recites "the insulative housing includes a first single-piece housing portion and a second single-piece housing portion" and "the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface." *Shin et al.* fails to teach or suggest this approach. Plastic encapsulating part 40 is a single-piece. Furthermore, claim 1 as amended herein includes the limitations of original claim 2, which was not rejected over *Shin et al.* Thus, the Examiner apparently recognizes that these limitations distinguish over *Shin et al.*

Claim 11 recites "the insulative housing consists of a first single-piece housing portion and a second single-piece housing portion" and "the first single-piece housing portion contacts the lower surface and the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal." *Shin et al.* fails to teach or suggest this approach. Plastic encapsulating part 40 is a single-piece. Furthermore, claim 11 as amended herein includes the limitations of original claim 12, which was not rejected over *Shin et al.* Thus, the Examiner apparently recognizes that these limitations distinguish over *Shin et al.*

Accordingly, claims 1, 5-11 and 17-20 distinguish over *Shin et al.*, and the amendments to claims 1 and 11 render the outstanding rejections moot.

The dependent claims recite additional distinctions over *Shin et al.* Some but not all of these distinctions are discussed below.

Claim 10 recites "the device is devoid of wire bonds, TAB leads and solder joints." Claim 20 recites similar limitations. *Shin et al.* fails to teach or suggest this approach. For instance, package 10α includes wire bonds 30, and package 10β includes solder joints 31 or wire bonds. In sustaining this rejection, the Examiner asserts that *Shin et al.* discloses in Figs. 1A, 1B

and 10B the device being devoid of wire bonds, TAB leads and solder joints. This is clearly erroneous. Figs. 1A and 1B merely disclose lead frame 1, which is not a device that includes a semiconductor chip and an insulative housing. Fig. 10B discloses lead 2 electrically connected to chip 20 by solder joint 31.

Under 35 U.S.C. § 102, anticipation requires that each and every element of the claimed invention be disclosed in the prior art. *Akzo N.V. v. United States International Trade Commission*, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986), *cert. denied*, 482 U.S. 909 (1987). That is, the reference must teach every aspect of the claimed invention. See M.P.E.P. § 706.02.

Shin et al. fails to teach or suggest limitations of independent claims 1 and 11 as well as limitations of various rejected dependent claims. Therefore, Applicant requests that these rejections be withdrawn.

IV. SECTION 103 REJECTIONS – SHIN ET AL. AND NAKAMURA ET AL.

Claims 2-4, 12-16 and 21-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shin et al.* in view of *Nakamura et al.* (U.S. Patent No. 5,405,809).

Nakamura et al. discloses a semiconductor device that includes light-transmitting substrate 1, circuit conductor layer 2, plated metal layer 3, metal bump 4, semiconductor chip 6, resin coating 7 and resin layer 8. Semiconductor chip 6 includes electrode 5.

Metal bump 4 is a metal such as Au that is formed on electrode 5 by plating or ball bonding, and then semiconductor chip 6 is cut out from a silicon wafer.

Circuit conductor layer 2 is a metal such as Cu or Al that is formed on light-transmitting substrate 1. For instance, circuit conductor layer 2 may be formed by depositing a metal layer on light-transmitting substrate 1 by sputtering, vapor deposition and the like and then patterning the metal layer using photolithography. Alternatively, circuit conductive layer 2 may be formed by attaching a flexible printed wiring board to light-transmitting substrate 1 or by thick-film printing.

Plated metal layer 3 is then formed on a prescribed portion of circuit conductor layer 2.

Resin layer 8 is then applied to a prescribed portion of light-transmitting substrate 1, and then semiconductor chip 6 is disposed face-down on resin layer 8 so that plated metal layer 3 abuts electrode 5. While semiconductor chip 6 is pressed onto light-transmitting substrate 1, resin layer 8 is irradiated with ultra violet rays through light-transmitting substrate 1 and partially cured.

The structure is then placed in an oven that melts plated metal layer 3 and further cures resin layer 8. Plated metal layer 3 melts and recoagulates so that alloy layers are formed in abutting portions between circuit conductor layer 2 and plated metal layer 3, and in abutting portions between plated metal layer 3 and metal bump 4.

Finally, resin coating 7 such as silicon is dispensed on light-transmitting substrate 1 and semiconductor chip 6.

Claim 1 (amended herein to recite the limitations of original claim 2) recites "an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion" and "the first single-piece housing portion contacts the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal."

Shin et al. fails to teach or suggest this approach. Plastic encapsulating part 40 does not include a first single-piece housing portion that contacts lead 2 and is spaced from lead end 4 and a second single-piece housing portion that contacts the first single-piece housing portion and lead end 4. Instead, plastic encapsulating part 40 is a single-piece that contacts lead 2 and lead end 4. *Nakamura et al.* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Shin et al.* using the assembly technique taught by *Nakamura et al.*, particularly since the proposed modification would render *Shin et al.* inoperative.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 2, Shin et al. discloses the claimed invention except for the insulative housing including a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) including a first single-piece housing portion (7) that contacts the lead (2) and is spaced from the terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55-57).

The rejection is flawed. There is no teaching, suggestion or motivation for the proposed modification.

Nakamura et al. discloses depositing circuit conductor layer 2 on light transmitting substrate 1, then depositing resin layer 8 on circuit conductor layer 2 and light-transmitting substrate 1, then disposing semiconductor chip 6 face-down on resin layer 8 such that light-transmitting substrate 1 provides the bottom surface, then curing resin layer 8, and then providing resin coating 7. If *Shin et al.* were assembled in this manner then lead end 4 would contact light-transmitting substrate 1 on the side opposite the bottom surface. That is, light-transmitting substrate 1 would prevent lead end 4 from extending to the bottom surface or being exposed. Instead, lead end 4 would be buried beneath light-transmitting substrate 1. This would render *Shin et al.* inoperative. Therefore, *Nakamura et al.* fails to teach or suggest that plastic encapsulating part 40 can be replaced by resin coating 7 and resin layer 8.

The Examiner states that the motivation for the proposed modification is to provide a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device. This is clearly erroneous. There is no motivation for a proposed modification that renders the reference inoperative.

Claim 11 (amended herein to recite the limitations of original claim 12) recites "the insulative housing consists of a first single-piece housing portion and a second single-piece housing portion" and "the first single-piece housing portion contacts the lower surface and the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal."

Shin et al. fails to teach or suggest this approach. Plastic encapsulating part 40 does not include a first single-piece housing portion that contacts the lower surface of chip 20, lead 2 and is spaced from lead end 4 and a second single-piece housing portion that contacts the first single-piece housing portion and lead end 4. Instead, plastic encapsulating part 40 is a single-piece that contacts the lower surface of chip 20, lead 2 and lead end 4. *Nakamura et al.* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Shin et al.* using the assembly technique taught by *Nakamura et al.*, particularly since the proposed modification would render *Shin et al.* inoperative.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 12, Shin et al. discloses the claimed invention except for the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) consists of a first single-piece housing portion (7) that contacts the lower surface and the lead (2) and is spaced from the terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary

artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55-57).

The rejection is flawed. There is no teaching, suggestion or motivation for the proposed modification, as explained above for claim 1.

Claim 21 recites "an insulative housing with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion."

Shin et al. fails to teach or suggest this approach. Plastic encapsulating part 40 does not include a peripheral portion that protrudes downwardly from a central portion. Instead, plastic encapsulating part 40 has a flat bottom surface. *Nakamura et al.* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Shin et al.* using the assembly technique taught by *Nakamura et al.*, particularly since the proposed modification would render *Shin et al.* inoperative.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 21, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36~40 a semiconductor package device, comprising:
> - an insulative housing (40) with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces;
> - a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;
> - a terminal (4 and 4') that protrudes downwardly from and extends through a central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad;
> - a lead (2) that protrudes laterally from and extends through

one of the side surfaces and is electrically connected to the pad;

- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclosure the bottom surface including a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion. However, Nakamura et al. discloses in Fig. 1 a bottom surface (A) including a peripheral portion (B) adjacent to the side surfaces and a central portion (area of 8) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protruding downwardly from the central portion. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shin et al. by using the peripheral portion as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55-57).

The rejection is flawed for several reasons.

First, there is no teaching, suggestion or motivation for the proposed modification, as explained above for claim 1.

Second, even if the proposed modification were made (although there is no teaching, suggestion or motivation to do so), the proposed modification would not meet the claim limitations.

Claim 21 recites that the peripheral portion protrudes downwardly from the central portion. In *Nakamura et al.*, resin coating 7 does not protrude downwardly from resin layer 8. Instead, resin coating 7 and resin layer 8 are bounded by light-transmitting substrate 1.

Claim 31 recites "an insulative housing with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion" and "a terminal that protrudes downwardly from and extends through the central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad, wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance."

Shin et al. fails to teach or suggest this approach. Plastic encapsulating part 40 does not include a peripheral portion that protrudes downwardly from a central portion. Instead, plastic encapsulating part 40 has a flat bottom surface. *Nakamura et al.* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Shin et al.* using the assembly technique taught by *Nakamura et al.*, particularly since the proposed modification would render *Shin et al.* inoperative.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 31, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36~40 a semiconductor package device, comprising:
> - an insulative housing (40) with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces;
> - a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
> - a terminal (4 and 4') that protrudes downwardly from and extends through a central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad;
> - a lead (2) that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the

pad;

- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclosure the bottom surface including a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion and wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance. However, Nakamura et al. discloses in Fig. 1 and Fig. 4 a bottom surface (A) including a peripheral portion (B) shaped as a rectangular ledge adjacent to the side surfaces and a recessed central portion (area of 8) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion and wherein a terminal (4) extends a second distance below the central portion, and the first distance is greater than the second distance. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shin et al. by using the peripheral portion as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55-57).

The rejection is flawed for several reasons.

First, there is no teaching, suggestion or motivation for the proposed modification, as explained above for claim 1.

Second, even if the proposed modification were made (although there is no teaching, suggestion or motivation to do so), the proposed modification would not meet the claim limitations.

Claim 31 recites that the peripheral portion protrudes downwardly from the central portion. In *Nakamura et al.*, resin coating 7 does not protrude downwardly from resin layer 8. Instead, resin coating 7 and resin layer 8 are bounded by light-transmitting substrate 1.

The Examiner states that resin coating 7 protrudes downwardly from resin layer 8. This is clearly erroneous.

Claim 31 also recites that peripheral portion extends a first distance below the central portion, the terminal extends a second distance below the central portion, and the first distance is greater than the second distance.

The Examiner states that metal bump 4 extends below resin layer 8. This is clearly erroneous. Metal bump 4 is coplanar with resin layer 8 at plated metal layer 3. Furthermore, even if metal bump 4 extended below resin layer 8 (although it does not), this is irrelevant to the proposed modification of replacing plastic encapsulating part 40 in *Shin et al.* with resin coating 7 and resin layer 8 in *Nakamura et al.*

Accordingly, claims 1, 11, 21 and 31 distinguish over *Shin et al.* in view of *Nakamura et al.*

The dependent claims recite additional distinctions over *Shin et al.* in view of *Nakamura et al.* Some but not all of these distinctions are discussed below.

Claim 2 recites "the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface." Claims 13, 23 and 33 recite similar limitations. *Shin et al.* fails to teach or suggest this approach, and *Nakamura et al.* fails to cure this deficiency, as explained above for claim 1.

Claim 22 recites "the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal."

Claims 32 and 44 recite similar limitations. *Shin et al.* fails to teach or suggest this approach, and *Nakamura et al.* fails to cure this deficiency, as explained above for claim 1.

Claim 26 recites "the peripheral portion of the bottom surface protrudes a first distance below the central portion of the bottom surface, the terminal protrudes a second distance below the central portion of the bottom surface, and the first distance is greater than the second distance." *Shin et al.* fails to teach or suggest this approach, and *Nakamura et al.* fails to cure this deficiency, as explained above for claim 31.

Claim 30 recites "the device is devoid of wire bonds, TAB leads and solder joints." Claim 40 recites similar limitations. *Shin et al.* fails to teach or suggest this approach, and *Nakamura et al.* fails to cure this deficiency, as explained above for claim 10.

To establish prima facie obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. See M.P.E.P. § 2142.

It is insufficient that the prior art shows similar components unless it also contains some teaching, suggestion or incentive for arriving at the claimed structure. See *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934 (Fed. Cir. 1990).

Moreover, if the proposed modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. See M.P.E.P. § 2143.01.

Shin et al. fails to teach or suggest limitations of independent claims 1, 11, 21 and 31 as well as limitations of various rejected dependent claims, and *Nakamura et al.* fails to cure these deficiencies. There is no teaching, suggestion or motivation to make the proposed modification, particularly since the proposed modification would render *Shin et al.* unsatisfactory for its intended purpose. Furthermore, the proposed modification would not meet the limitations of claims 21 and 31. Therefore, Applicant requests that these rejections be withdrawn.

V. SECTION 103 REJECTIONS – SHIN ET AL. AND KURAISHI ET AL.

Claims 41, 45-51 and 57-60 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shin et al.* in view of *Kuraishi et al.* (U.S. Patent No. 5,859,471).

Kuraishi et al. addresses TAB leads with insufficient outer lead strength:

> However, as mentioned above, since a TAB tape includes a plurality of leads which are made of conductive thin film, there has been a problem that the leads are not of sufficient strength and it is difficult to handle same, such as when the product is mounted on a printed circuit board. (Col. 1, lines 48-52.)
>
> In addition, after the leads have been formed, it is necessary to prevent the leads from being deformed or bent. Thus, it becomes necessary that the outer leads have a certain strength to stably and accurately mount the product on a printed circuit board without any deformation of the leads. (Col. 1, lines 58-63.)

Kuraishi et al. solves the problem by coating the outer leads to increase the strength of the outer leads:

> According to one aspect of the present invention . . . said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained. (Col. 2, lines 5-13.)
>
> According to another aspect of the present invention . . . said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained. (Col. 2, lines 14-23.)

According to still another aspect of the present invention . . . coating said outer leads with metal layers to increase the thickness of said outer leads, so that a desired strength of said outer leads is obtained. (Col. 2, lines 24-34.)

According to further aspect of the present invention . . . coating said outer leads with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained. (Col. 2, lines 35-48.)

According to still further aspect of the present invention . . . coating said outer leads with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained. (Col. 2, lines 49-63.)

According to still another aspect of the present invention . . . said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained. (Col. 2, line 64 to col. 3, line 5.)

According to still another aspect of the present invention . . . said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained. (Col. 3, lines 9 to 22.)

According to still another aspect of the present invention . . . said outer leads being coated with metal layers to increase the thickness thereof, so that a desired strength of said outer leads is obtained. (Col. 3, lines 27 to 39.)

Kuraishi et al. discloses a TAB tape lead frame that includes base film 10 and a conductive pattern. Base film 10 includes window holes 14 and sprocket holes 16. The conductive pattern includes inner leads 18 and outer leads 20.

In an inner lead bonding type TAB tape shown in Figs. 1A and 1B, base film 10 includes device hole 12. In a wire bonding type TAB tape shown in Figs. 1C and 1D, the conductive pattern includes die pad 28. Both types of TAB tape can include tie bar 20a shown in Figs. 1B and 1D.

Outer leads 20 are subsequently plated with copper to increase strength:

> In each of the above types of TAB tapes, the thickness of the conductive part of the outer lead is increased, in such a manner that the outer lead has a thickness substantially the same as the outer lead of a conventional lead frame. . . . As the thickness of outer leads 20 is increased, as shown in FIGS. 3 and 4, by the copper-plating, the strength can also be increased to substantially the same level as a conventional metal lead frame. (Col. 5, lines 5-19.)
>
> As shown in FIGS. 3 and 4, the thickness of the outer leads 20 is increased by copper-plating, so that the strength of the outer leads 20 is substantially the same as that of a conventional metal lead frame. Therefore, the outer lead portions 20 can easily be handled, and bent, so that the semiconductor device using such a lead frame of the embodiments can easily be mounted on a circuit board (not shown). (Col. 5, line 66 to col. 6, line 6.)

Claim 41 recites "a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that contacts and extends into the insulative housing and is spaced from the top and bottom surfaces and does not overlap the chip and a non-recessed portion that contacts and extends outside the insulative housing and is adjacent to the recessed portion and the bottom surface." *Shin et al.* fails to teach or suggest this approach. Lead 2 does not include a lead that protrudes laterally from and extends through a side surface of plastic encapsulating part 40, includes a recessed portion that contacts and extends into plastic encapsulating part 40 and is spaced from the top and bottom surface and does not overlap the chip, includes a non-recessed portion that contacts and extends outside plastic encapsulating part 40 and is adjacent to the recessed portion and the bottom surface, is spaced and separated from lead end 4 outside plastic encapsulating part 40, and is electrically connected to lead end 4 inside plastic encapsulating part 40 and outside chip 20. *Kuraishi et al.* fails to cure this deficiency. Even if *Shin et al.* was modified by coating lead 2 to increase strength as taught by *Kuraishi et al.*, the proposed modification would not meet the claim limitations since the portion of lead 2 exposed at the side surface of plastic encapsulating part 40 would not be adjacent to the bottom surface of plastic encapsulating part 40 through which lead end 4 protrudes.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 41, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36~40 a semiconductor package device, comprising:
> - an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
> - a semiconductor chip (20) within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;
> - a terminal (4) that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and
> - a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad;
> - wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.
>
> Shin et al. does not disclose the lead includes a recessed portion. However, Kuraishi et al. discloses in Fig. 4 the lead including a recessed portion (upper part of 18) that extends through a side surface and is spaced from the top and bottom surfaces and a non-recessed portion (20) that extends outside an insulative housing (26) and is adjacent to the recessed portion. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shin et al. by using the peripheral portion as taught by Kuraishi et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a semiconductor device that can easily be mounted on a printed circuit board (column 2, lines 3 and 4).
>
> A further difference between Shin et al., as modified, and claimed invention is a non-recessed portion of the lead being located at a corner between a side surface and a bottom surface. However, such a difference is regard as nothing more than obvious design variation of Shin et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the non-recessed portion of the lead at the location of a "corner between a side surface and a bottom surface." The ordinary artisan would have been motivated to

further modify Shin et al. in the manner described above for at least the purpose of decreasing manufacture cost by decreasing number of lead bending.

The rejection is flawed. There is no teaching, suggestion or motivation for the proposed modification.

Shin et al. fails to teach or suggest bending a portion of lead 2 that protrudes from the side surface of plastic encapsulating part 40 such that the bent-around portion of lead 2 is adjacent to the bottom surface of plastic encapsulating part 40. Furthermore, *Shin et al.* teaches away from this approach. Lead ends 4 are distributed as a compact grid array at the bottom surface of plastic encapsulating part 40. Providing lead 2 with a bent-around portion adjacent to the bottom surface would serve no purpose since lead 2 already includes lead end 4 at the bottom surface within a compact grid array. Furthermore, providing lead 2 with a bent-around portion adjacent to the bottom surface would provide less efficient heat emission than if the bent-around portion was spaced from the bottom surface, as shown in Fig. 20.

Kuraishi et al. fails to teach or suggest bending outer lead 20 so that outer lead 20 is adjacent to the bottom surface of mold resin 26.

Thus, neither *Shin et al.* nor *Kuraishi et al.*, alone or in combination, teach or suggest this approach.

The Examiner asserts the proposed modification is "an obvious design variation of Shin et al." This is clearly erroneous. *Shin et al.* fails to teach or suggest this approach, and there is no apparent reason why one skilled in the art would pursue it.

The Examiner states that the motivation for the proposed modification is "decreasing manufacture cost by decreasing number of lead bending." This is clearly erroneous. Furthermore, this is illogical and confusing. What does "decreasing number of lead bending" mean? How would this position the lead adjacent to the bottom surface? How would this decrease manufacturing cost?

Claim 51 recites "a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that contacts and extends into the insulative housing and is spaced from the top and bottom surfaces and does not overlap the chip and a non-recessed portion that contacts and extends outside the insulative housing and is adjacent to the recessed portion and the bottom surface, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip." *Shin et al.* fails to teach or suggest this approach, and *Kuraishi et al.* fails to cure this deficiency, as explained above for claim 41.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 51, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36~40 a semiconductor package device, comprising:
> - an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
> - a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad (31), the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
> - a terminal (4 and 4') that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and
> - a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad;
> - wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.
>
> Shin et al. does not disclose the lead includes a recessed portion. However, Kuraishi et al. discloses in Fig. 4 the lead including a recessed portion (upper part of 18) inside an insulative housing that extends through a side surface and is spaced from the top and bottom surfaces and a non-recessed portion (20) outside an insulative housing that is adjacent to and integral with the recessed

> portion and contacts the side surface. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shin et al. by using the peripheral portion as taught by Kuraishi et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a semiconductor device that can easily be mounted on a printed circuit board (column 2, lines 3 and 4).
>
> A further difference between Shin et al., as modified, and claimed invention is a non-recessed portion of the lead being adjacent to at a corner between a side surface and a bottom surface. However, such a difference is regard as nothing more than obvious design variation of Shin et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the non-recessed portion of the lead at the location of a "corner between a side surface and a bottom surface." The ordinary artisan would have been motivated to further modify Shin et al. in the manner described above for at least the purpose of decreasing manufacture cost by decreasing number of lead bending.

The rejection is flawed. There is no teaching, suggestion or motivation for the proposed modification, as explained above for claim 41.

Accordingly, claims 41, 45-51 and 57-60 distinguish over *Shin et al.* in view of *Kuraishi et al.*

The dependent claims recite additional distinctions over *Shin et al.* in view of *Kuraishi et al.* Some but not all of these distinctions are discussed below.

Claim 50 recites "the device is devoid of wire bonds, TAB leads and solder joints." Claim 60 recites similar limitations. *Shin et al.* fails to teach or suggest this approach, and *Kuraishi et al.* fails to cure this deficiency, as explained above for claim 10.

To establish prima facie obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the

prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. See M.P.E.P. § 2142.

It is insufficient that the prior art shows similar components unless it also contains some teaching, suggestion or incentive for arriving at the claimed structure. See *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934 (Fed. Cir. 1990).

Moreover, if the proposed modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. See M.P.E.P. § 2143.01.

Shin et al. fails to teach or suggest limitations of independent claims 41 and 51 as well as limitations of various rejected dependent claims, and *Kuraishi et al.* fails to cure these deficiencies. There is no teaching, suggestion or motivation to make the proposed modification, particularly since the proposed modification is based on unsupported and illogical notions of motivation. Therefore, Applicant requests that these rejections be withdrawn.

VI. SECTION 103 REJECTIONS – SHIN ET AL., KURAISHI ET AL. AND NAKAMURA ET AL.

Claims 42-44 and 52-56 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shin et al.* in view of *Kuraishi et al.* and *Nakamura et al.*

Claim 42 recites "the insulative housing includes a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal ." *Shin et al.* fails to teach or suggest this approach, and *Nakamura et al.* fails to cure this deficiency, as explained above for claim 1. Furthermore, claim 42 depends from claim 41, which distinguishes over *Shin et al.* in view of *Kuraishi et al.*, as explained above for claim 41.

Claim 52 recites "the insulative housing consists of a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal ." *Shin et al.* fails to teach or suggest this approach, and *Nakamura et al.* fails to cure this deficiency, as explained above for claim 11. Furthermore, claim 52 depends from claim 51, which distinguishes over *Shin et al.* in view of *Kuraishi et al.*, as explained above for claim 51.

Claim 53 recites "the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface." *Shin et al.* fails to teach or suggest this approach, and *Nakamura et al.* fails to cure this deficiency, as explained above for claim 1. Furthermore, claim 53 depends from claim 51, which distinguishes over *Shin et al.* in view of *Kuraishi et al.*, as explained above for claim 51.

Therefore, Applicant requests that these rejections be withdrawn.

VII. NEW CLAIMS

Claims 61-120 have been added to further explicate various features of the invention. No new matter has been added.

Claim 61 recites "a routing line within the insulative housing that overlaps and is electrically connected to the pad" and "a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad" and "a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through the side surface and is electrically connected to the pad." *Shin et al.* fails to teach or suggest this approach. Lead 2 does not include a non-integral routing line and lead as claimed. Claims 62-70 depend from claim 61.

Claim 71 recites "a routing line within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad" and "a terminal that protrudes

downwardly from and is integral with the routing line, protrudes downwardly from and extends through the bottom surface, is spaced from the side surface and is electrically connected to the pad" and "a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through the side surface and is electrically connected to the pad." *Shin et al.* fails to teach or suggest this approach. Lead 2 does not include a non-integral routing line and lead as claimed. Claims 72-80 depend from claim 71.

Claim 81 recites "a routing line within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad" and "a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the central portion of the bottom surface, is spaced from the side surfaces and is electrically connected to the pad" and "a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through one of the side surface and is electrically connected to the pad." *Shin et al.* fails to teach or suggest this approach. Lead 2 does not include a non-integral routing line and lead as claimed. Claims 82-90 depend from claim 81.

Claim 91 recites "a routing line within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad" and "a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the central portion of the bottom surface, is spaced from the side surfaces and is electrically connected to the pad" and "a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through one of the side surface and is electrically connected to the pad." *Shin et al.* fails to teach or suggest this approach. Lead 2 does not include a non-integral routing line and lead as claimed. Claims 92-100 depend from claim 91.

Claim 101 recites "a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed

portion and contacts the insulative housing, the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the bottom surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the bottom surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another." *Shin et al.* fails to teach or suggest this approach, and *Kuraishi et al.* fails to cure this deficiency. In *Shin et al.*, even if a coating was deposited on lead 2 as taught by *Kuraishi et al.* such that lead 2 included a recessed portion and a non-recessed portion, all four of the outer surfaces of the recessed and non-recessed portions would not be coplanar with one another where the recessed and non-recessed portions are adjacent to one another. Claims 102-110 depend from claim 101.

Claim 111 recites "a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulative housing, the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the bottom surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the bottom surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another." *Shin et al.* fails to teach or suggest this approach, and *Kuraishi et al.* fails to cure this deficiency. In *Shin et al.*, even if a coating was deposited on lead 2 as taught by *Kuraishi et al.* such that lead 2 included a recessed portion and a non-recessed portion, all four of the outer surfaces of the recessed and non-recessed portions would not be coplanar with one another where the recessed and non-recessed portions are adjacent to one another. Claims 112-120 depend from claim 111.

VIII. OTHER DRAWING CHANGES

In Fig. 2A, reference character 132 only points to the recessed portion. However, the Examiner objected to a similar feature in U.S. Application Serial No. 10/082,500 filed February 25, 2002, which is a continuation-in-part of the captioned-application. Therefore, in the interests of expediting the case, the Submission Of Proposed Drawing Amendment For Approval By Examiner filed concurrently herewith proposes straightening the lead line for reference character 132 in Fig. 2A.

In Fig. 6B, reference character 156 should point to the encapsulant, and the Examiner objected to a similar feature in U.S. Application Serial No. 10/082,500 filed February 25, 2002, which is a continuation-in-part of the captioned-application. Therefore, in the interests of expediting the case, the Submission Of Proposed Drawing Amendment For Approval By Examiner filed concurrently herewith proposes that reference character 156 point to the encapsulant in Fig. 6B.

In Fig. 10C, routing line 148 overlaps but does not contact pad 116. However, the Examiner objected to a similar feature in U.S. Application Serial No. 10/082,500 filed February 25, 2002, which is a continuation-in-part of the captioned-application. Therefore, in the interests of expediting the case, the Submission Of Proposed Drawing Amendment For Approval By Examiner filed concurrently herewith proposes showing adhesive 154 between routing line 148 and pad 116 in Fig. 10C.

IX. OTHER AMENDMENTS

The Specification and Claims have been amended to improve clarity. No new matter has been added.

X. PRELIMINARY AMENDMENT

A Preliminary Amendment was filed on April 25, 2003 – two days after the outstanding Office Action was mailed, and one day before the outstanding Office Action was received. As a result, the Preliminary Amendment was not filed before the outstanding Office Action and should not be entered.

Applicant withdraws the Preliminary Amendment.

XI. FEES

The fee for this Response is calculated below:

For	Claims Remaining After Amendment	Highest Number Previously Paid For		Extra Claims	Rate		Additional Fee
Total Claims	120	– 60	=	60	x $9	=	$540
Independent Claims	12	– 6	=	6	x $42	=	$252
Multiple Dep. Claim	0	0				=	0
Total Fee						=	$792

Please charge the $792 fee to Deposit Account No. 502178/BDG005 and charge any underpayment or credit any overpayment to this Account.

XII. CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

The application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 5, 2003.

D Sigmond — 5,5,03

David M. Sigmond
Attorney for Applicant

Date of Signature

Respectfully submitted,

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